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EXPERIENCE

October 2013 to Present

Iron Heart Consulting, LLC – Founder and Principal

Provide engineering consulting services for technology companies at all stages and sizes, which encompass hardware, software, project management, technical communications, and evaluating organizational management effectiveness (i.e., troubleshooting). Services range from conceptual design and project planning to final project sign-off. Current clients include:

- *Graphite Systems Inc*., startup company based in Mountain View, CA: Director, Systems Hardware Engineering. March 2014 to present.
- *Contec Holdings, LLC*, telecommunications company based in Schnectady, NY: Architect and Manager, Systems Hardware Engineering. October 2013 to present.
- *ViaSat Inc.*, telecommunications company based in Carlsbad, CA: Advise on possible IP for LDPC in flash storage systems. April 2014 to present.

January 2010 to October 2013

Violin Memory – Senior Vice President of Engineering

Managed overall product development and quality, which included:

- Hiring and managing an engineering department that grew from 14 to 200 people, including 20 managers at various levels and two vice presidents; and from a budget of $10 million to $51 million.
- Creating and developing a complete engineering department structure, including hardware development, software development, QA, technical publications, CAD design, and software release management.
- Overseeing the acquisition and integration of two companies (Gear6 and Gridiron).
- Collaborating with the CTO to determine the technologies, functions, and features of the flagship flash Memory Array product lines.
- Managing the design and introduction of the flash Virtual Array products, which generated $100 million of revenue in their first year.
- Working directly with customers to integrate products into their organizations, including understanding their requirements.
- Establishing relationships with major vendors, including Toshiba and Altera.
- Participating in the solicitation and recruitment of senior executives.

2008-2010

Seamicro – Vice President of Engineering

Provided engineering leadership that resulted in successful prototype deployment at customer sites.

- Oversaw all aspects of staffing, scheduling, budgeting, vendor selections, and Beta programs.
- Directly managed software, systems hardware, and chip design staffs.
- Developed methods and processes relating to the scheduling, specification, and implementation of features.
- Worked with product marketing to determine features and their priority.
- Hired additional staff as needed to achieve schedule and functional goals.
- Worked with CTO to implement technology, and resolve technology problems.

2002-2008 Mistletoe Technologies (AKA Gigafin Networks) – CTO and Co-Founder

- Developed full 1GE packet processing chip, including all elements for IPSEC-style VPN. Designs using the chip produced a 10X improvement in power and performance. Chip parameters – 961 pins, TSMC 130um, 12 x 13 m die, and 9 watts power.
- Pioneered the use of hardware parsing for packet processing, coupled with direct execution flows.
- Built network appliance products for DDoS protection, internet firewalls, and network security analysis. Customers included University of Illinois, Dominic University in San Rafael, and these Korean Internet Data Centers: KT, Hanaro, CDNetworks, UBDIGM.

1999-2002 Force10 Networks – Director, Systems Engineering

Hired and managed an engineering team to design, bringup, and ship all the chassis and board products for a large scale 10Gbps Ethernet switch/router.

- Managed a budget of $14 million and a staff of 55 people, including four managers.
- Staff included design engineers, PCB engineers, mechanical, power and thermal engineers, diagnostic software engineers, and signal integrity engineers.
- Product shipped on time and met Beta customers' expectations.
- Additionally, provided system architectural support to CTO.

1998-1999 CacheFlow (now Blue Coat Systems) – Hardware Design Engineer

- Architect and Hardware Designer for an L4 100Mbps Ethernet switch.
- Bringup and release to manufacturing of the 5000 and 3000 Web Cache product.

1993-1998 Cisco Systems, Inc. – Data Communications Engineer

- *Engineering Manager* - Technologies and ASIC Group - Access Business Unit - 25 person staff, budget of $6.8 million. Founded VoIP endeavor for Cisco. Developed four ASICs, including router on a chip.
- Developed 16 bit wide instruction set for MIPS processor (TINYRISC – MIPS16).
- *Engineering Project Lead* - architect for 1000, 1600, and 3600 families of low-end routers.
- Reviewed companies for business development group, made recommendations as to potential and applicability to Cisco products and direction. Served on Patent Council.

1987-1993 Tandem Computers – Data Communications Engineer

1986-1987 Boeing – Communications Engineer

1977-1986 IBM – Contract support/development

PRESENTATIONS AND PATENTS

- Implications of using Flash devices in an enterprise storage server. Presented at Hot Chips, A Symposium on High Performance Chips, Stanford, CA August 2013.
- "Fault Tolerant Connection of a computing system to a local area network" – 5,448,723
- "Apparatus and Method for a Network Router – Router on a Chip" – 5,991,817
- "Method for dual use - fast access to a PCMCIA Flash memory card" – 6,148,347
- "signaling state management system for network gateways" – 6,188,760
- "Network router integrated onto a silicon chip" – 6,366,583
- "signaling state management system for packet network gateways" – 6,411,705
- "reconfigurable semantic processor" – 7,130,987
- "semantic processor storage server architecture" - 7,251,722

- "network router integrated onto a silicon chip" – 7,324,546
- "contextual memory interface for network processor" – 7,398,356
- "Parser table/production rule table configuration using CAM and SRAM" – 7,415,596
- "Array machine context data memory" – 7,424,571
- "Arbiter for array machine context data memory" – 7.451.268
- "Symbol parsing architecture" – 7,478,223

EDUCATION 1977 - University of Oklahoma – BS, Math